Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **1CLK**
2. **1K**
3. **1J**
4. **1PRE**
5. **1Q**
6. **1Q**
7. **2Q**
8. **GND**
9. **2Q**
10. **2PRE**
11. **2J**
12. **2K**
13. **2CLK**
14. **2CLR**
15. **1CLR**
16. **VCC**

**.059”**

**14 13 12**

**11**

**10**

**9**

**8**

**7**

**3 4 5 6**

**15**

**16**

**1**

**2**

**MASK**

**REF**

**112**

**.067”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential: VCC or FLOAT**

**Mask Ref: 112**

**APPROVED BY: DK DIE SIZE .059” X .067” DATE: 2/21/23**

**MFG: SILICON SUPPLIES THICKNESS .014” P/N: 54HC112**

**DG 10.1.2**

#### Rev B, 7/1